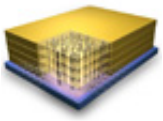

Altera and Micron Demonstrate Working Hybrid Memory Cube with FPGAs

Altera and Micron Show Off HMC Device with 160GB/s Memory Bandwidth

by **Anton Shilov**
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Altera Corp. and Micron Technology have jointly demonstrated successful interoperability between Altera Stratix V FPGAs and Micron's hybrid memory cube (HMC). This technology achievement enables system designers to evaluate today the benefits of HMC with FPGAs and SoCs for next-generation communications and high-performance computing designs.

Altera and Micron have developed a special demo board that features one Micron HMC short-reach (SR) device configured as a 2GB cube capable of 160GB/s of total bandwidth as well as four Altera Stratix V FPGAs (currently they are among the highest-performing FPGAs in the industry), each dedicated to one of HMC's four links, running at 10Gb/s lane rate, for full 160GB/s peak bandwidth capability. The demonstration board is supposed to show the exceptional memory bandwidth of Micron's HMC and Altera's abilities to support them. Actual applications that will take advantage of Micron's HMCs will be based on much more capable Arria 10 FPGAs and SoCs as well as Stratix 10 FPGAs and SoCs due to be available in 2014 and 2015, respectively.

"By demonstrating Stratix V and HMC working together now, we are enabling our customers to leverage their current development with Stratix V FPGAs and prepare for production deployment in Altera's Generation 10 devices, knowing they will have proven HMC support. The partnership between Altera and Micron to deliver this capability puts our customers at the forefront of innovation," said Danny Biran, senior vice president of marketing and corporate strategy at Altera.

HMC has been recognized by industry leaders and influencers as the long-awaited answer to address the limitations imposed by conventional memory technology, and provides ultra-high system performance with significantly lower power-per-bit. HMC delivers up to 15 times the bandwidth of a DDR3 module and uses 70% less energy and 90% less space than existing technologies. HMC's abstracted memory allows designers to devote more time leveraging HMC's features and performance and less time navigating the multitude of memory parameters required to implement basic functions. It also manages error correction, resiliency, refresh, and other parameters exacerbated by memory process variation. Micron expects to begin sampling HMC later this year with volume production ramping in 2014.

Arria 10 FPGAs and SoCs are the first device families in Altera's generation 10 portfolio and will be the first devices to support HMC technology in volume production. Made using 20nm process technology at TSMC, Arria 10 FPGAs and SoCs will use HMC to extend the benefits by providing both 15% higher core performance than today's highest performance Stratix V FPGAs and up to 40% lower power compared to the lowest power Arria V midrange FPGAs. Arria 10 FPGAs and SoCs will offer up to 96 transceiver channels, enabling customers to take full advantage of the bandwidth that HMC has to offer. First samples of Arria 10 devices will be available in early 2014, with Quartus II design software support available now in early access.

Stratix 10 FPGAs and SoCs are expected to enable the most advanced, highest performance applications across communications, military, broadcast and compute and storage markets. These high-performance applications often require the highest memory bandwidth, which drives the need for an HMC-ready architecture. Made using Intel Corp.'s 14nm process technology, Stratix 10 FPGAs and SoCs will enable system solutions with an operating frequency over one gigahertz, and two times the core performance of current high-end 28 nm FPGAs. Stratix 10 devices will also allow customers to achieve up to a 70% reduction in power consumption at performance levels equivalent to the previous generation. Altera will have 14 nm Stratix 10 FPGA test chips in 2013 and design software support in 2014.