Fujitsu uses HMC tech in petascale computing

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November 2013 – The high bandwidth memory technology recently introduced to the market by Micron – the Hybrid Memory Cube (HMC) – has made its way into an early adopter system application – Supercomputers. In a joint announcement by Micron and Fujitsu, it was revealed that a new supercomputer prototype board design for next-generation systems will be unveiled at the Supercomputer '13 Conference in Denver, featuring sockets for the HMC memory solution.

A challenge for these systems is the requirement to address the tremendous data movement needs so the supercomputer's multi-core and multiprocessor architecture can reach high efficiency. These systems are bounded by the tradeoffs of form factor, total energy consumed (operational, heat, cooling), and total system bandwidth. The new system board being shown has sockets for 3 CPU ICs and 8 HMC sockets.

The HMC memory, which uses a common socket configuration for both the 2GB and 4GB initial product releases, delivers a 160GB/s of memory bandwidth at an operational energy that is 70% less than existing technologies. Yuji Oinaga, head of Fujitsu's Next Generation Technical Computing Unit stated "For optimal performance efficiency of the application software, it is essential to improve the B(Bytes)/F(Flops) ratio, and HMC represents the new standard in memory performance for supercomputing."

The HMC solution has been created by a multi-vendor consortium to address the growing gap between the performance improvement rate of DRAM and processor data consumption rates.

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