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## Micron Hybrid Memory Cube Aimed at HPC

*Volume production of 2GB and 4GB devices expected "later in 2014"*

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[Micron Technology, Inc.](#) is planning to adapt its [Hybrid Memory Cube](#) (HMC) for petascale supercomputer systems, representing a step forward in memory technology.

HMC is designed for applications requiring low-energy, high-bandwidth access to memory, which is

the important requirement for supercomputers. Other applications include data packet processing, data packet buffering or storage, and processor acceleration.

Micron and [Fujitsu Limited](#) will exhibit a display board that features HMC devices in Fujitsu's next-generation supercomputer prototype at the Supercomputing '13 Conference in Denver, CO, November 19-21.

Supercomputing is a technology that enables scientists and engineers to address complex simulations that drive R&D and enables them to explore fundamental questions about the organization of the universe. Addressing topics of this magnitude requires tremendous data movement capability. Using HMC to unlock the potential of a supercomputer's multicore processor architecture will enable performance efficiency.

*"The designers and engineers at Fujitsu saw early on the value of raising their system to the next level with the help of Hybrid Memory Cubes," said Brian Shirley, VP of Micron's DRAM solutions group. "We anticipate helping Fujitsu to immediately grow their capabilities for the most advanced computing challenges."*

*"Our system designers are highly impressed with HMC because it enables new memory system designs that support our increased demand for bandwidth, super-compact form factor, and optimized energy per bit," said Yuji Oinaga, head of Fujitsu's next generation technical computing unit. "For optimal performance efficiency of the application software, it is essential to improve the Bytes/Flops ratio, and HMC represents the new standard in memory performance for supercomputing."*

HMC uses advanced through-silicon vias (TSVs)-vertical conduits that electrically connect a stack of individual chips-to combine high-performance logic with Micron's DRAM. HMC delivers an **160GB/s of memory bandwidth** while using up to 70% less energy per bit than existing technologies, which lowers customers' TCO.

HMC was recently named *Memory Product of the Year* by *EDN* and *EE Times*.

Micron expects volume production of both the 2GB and 4GB HMC devices later in 2014.

#### **Read also:**

[Micron Ships First Samples of Hybrid Memory Cube](#)

2 and 4GB HMC shipping in mid 2014

[New Members at Hybrid Memory Cube Consortium](#)

ARM, HP, and SK Hynix

[IBM to Produce Micron Hybrid Memory Cube in East Fishkill, NY](#)

With bandwidth of 128GB/s

[Micron and Samsung Launch Consortium For New Memory](#)

Called Hybrid Memory Cube competing with DRAM

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