Micron Technology, Inc. (NASDAQ:MU) earns good praise for its Hybrid Memory Cube

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P ov 15 2013 - 9:27am *by* Benjamin Roussey

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Boston, MA, 11/15/2013 (wallstreetpr) – Micron Technology, Inc. (NASDAQ:M has announced that it is planning to adopt the Hybrid Memory Cube (HMC) f petscale supercomputers which marks a huge step for the company. The ne technology is planned for applications that require low energy, high bandwid access to memory, which is an important requirement for supercomputers.

The company and Fujitsu which is a global leader in the supercomputing indust will both exhibit a display board which will feature HMC devices in a prototy which will be a next generation supercomputer at the Supercomputing Conference which will be held in Denver between 19-21 Novembers.

Supercomputing is an important technology which allows scientists and enginee to tackle complex simulations that drive research and development and helps the to find out important questions about the organization of our world. Tacking su difficult questions need excellent data movement capability. Using the new devi to meet the ability of the supercomputer's multicore processor architecture w allow the supercomputer to function efficiently.

Brian Shirley, vice president of Micron's DRAM Solutions Group said that t designers and engineers at Fujitsu had recognized the potential of the HMC devi early and it expected that the company would be able to help the latter company grow its capabilities in the sector.

Yuji Oinaga, head of Fujitsu's Next Generation Technical Computing Unit said that

his company's designers were very happy with the HMC design.

HMC which is the latest breakthrough uses the latest through-silicon vias (TSV that connect chips stacked on top of each other electrically. It gives 160 GB memory bandwidth while using only 70% less energy per bit than the technologie already existing thus reducing the clients total cost of ownership (TCO).

The device has won recognition from leaders in the industry as the long waite reply to meet the growing gap between the DRAM performance rate and tl consumption rate of processor data.

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About the Auth

Benjamin Roussey is from Sacramento, California. He has two master's degrees and served four years i the U.S. Navy. His bachelor's degree is from CSUS (1999) where he was on a baseball pitching scholarship. His second master's degree is an MBA in Global Management from the University of Phoen (2006). He has worked for small businesses, public agencies, and large corporations. He has lived in Korea and Saudi Arabia where he was an ESL instructor. Benjamin spends his time in between Northerr California and Cabo San Lucas, Mexico, committing himself to his craft of freelance and website writing. http://www.facebook.com/ben.rouss

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