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Fujitsu guns for faster supercomputers with new chip

The company is targeting 100-petaflop supercomputers with the SPARC64 XIfx chip

By Agam Shah
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IDG News Service - The world's fastest computer is facing a challenge from Fujitsu, which is developing a new high-performance chip that could go into supercomputers up to three times faster.

Fujitsu's SPARC64 XIfx processor could be used in supercomputers capable of delivering performance of up to 100 petaflops, which is roughly three times the peak performance of the world's fastest computer, China's Tianhe 2 supercomputer, which has peak performance of 33.86 petaflops and uses Intel's Xeon E5 CPU and Xeon Phi co-processor.

The Japanese company is no stranger to delivering speedy chips. The new SPARC64 XIfx is two generations ahead of the eight-core SPARC64 VIIIfx processor, which is used in the world's fourth-fastest computer, called K. K. That supercomputer, located in Japan, delivers 11.28 petaflops of peak performance.

The SPARC64 XIfx will succeed the current SPARC64 IXfx, which is used in high-performance PrimeHPC FX10 servers sold by Fujitsu. The upcoming XIfx will offer performance of more than 1 teraflop, about four times its predecessor.

Fujitsu will present more details on the SPARC64 XIfx chip at next week's Hot Chips conference in Cupertino.

A petaflop equals 1,000 trillion floating point calculations per second. Countries are looking for faster supercomputers to remain technologically competitive in solving complex problems in areas like national security, economics and science. Supercomputers also help university researchers in areas like space, energy, meteorology and biological sciences.

The SPARC64 XIfx chip has 32 processor cores and an array of memory and throughput technologies that improve data transfers within the system and between servers, according to a paper on the company's website.

Twelve XIfx chips will fit into a 2U chassis, giving the server 384 main processing cores. Each chip also has two "assistant" cores in addition to the 32 main processing cores, according to the presentation. The function performed by the assistance cores isn't clear.

The throughput improvements will include on-board support for Hybrid Memory Cube, which is considered an upgrade from DRAM in servers today. HMC has

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memory modules stacked on top of each other, instead of lying flat next to each other on a motherboard. According to memory maker Micron, HMC provides 15 times more throughput and is 70 percent more power efficient than conventional DDR3 DRAM modules.

Data transfer improvements are also gained via the new Tofu 2 interconnect, which enables the CPU and other components to communicate with each other. The interconnect has a maximum speed of 12.5 gigabytes per second, around two-and-a-half times faster than its predecessor, Tofu 1, which is used in the K computer. Tofu 2 will be integrated and connect to the Xlfx CPU directly, which will reduce latency. The Tofu 1 interfaces are implemented in separate chips on the K computer and other Fujitsu servers.

Servers with the chip will also support optical interfaces, allowing servers to network using fiber optics, which is considered faster than copper cables.

Agam Shah covers PCs, tablets, servers, chips and semiconductors for IDG News Service. Follow Agam on Twitter at @agamsh. Agam's e-mail address is agam_shah@idg.com

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