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"Yes, Chipvision had an interesting system of just that type. I talked to them about it at the time, because we have an energy..." - *Grant Martin*

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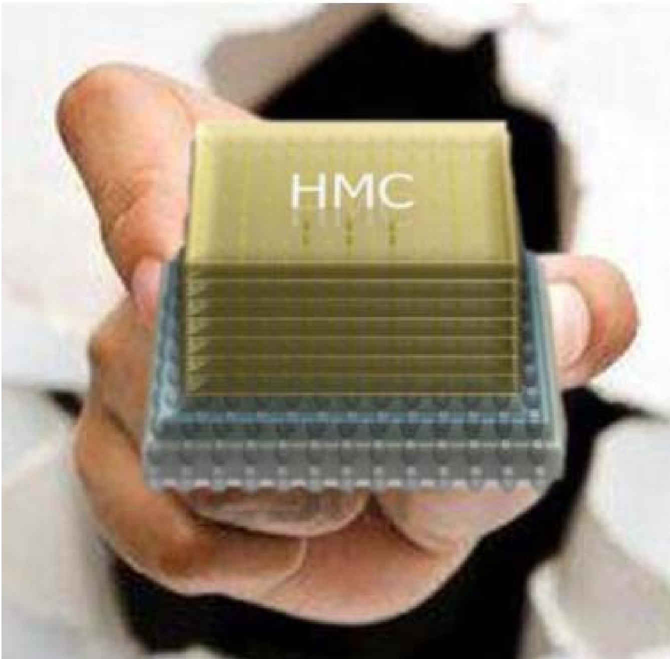
Samsung, Micron Unveil 3D Stacked Memory And Logic

By Ed Sperling
Samsung and Micron have joined forces to create 3D stacked memory, a development that has profound implications for manufacturing, packaging, design and power.

The fruit of their joint venture is the Hybrid Memory Cube—a hybrid of memory and logic—that comes in either four- or eight-layer stacks of memory. The logic layer is a memory controller that will work like a hypervisor for testing, routing and optimization.

The new device is a true 3D stack, including between 2,000 and 3,000 through-silicon vias. The die themselves will be manufactured at the 20nm process node or smaller, with an expected jump in throughput that will enable movement of the same amount of data for 70% less power, according to Scott Graham, general manager of DRAM marketing for Micron Technology.



Graham said the consortium will send invitations out to potential partners and that the specification for the HMC will be finalized next year. Still to be worked out is who manufactures the HMC. Both companies are expected to use different manufacturing facilities.

What becomes particularly interesting with 3D memory is the possibility of using the memory much more judiciously with heterogeneous cores so only the resources that are needed are actually used. That can save on power while also reserving enough performance for those applications that require more memory and processing power. These memories can be used both in 3D stacks, as well as 2.5D stacked configurations where the memory is connected through an interposer layer.

Both Graham and Pablo Temprano, director of DRAM and graphics marketing at Samsung Semiconductor, acknowledged there are numerous possible scenarios for using this technology. They noted that some customers also are looking at using 3D stacked memory to replace some of the cache on a chip because moving data in and out of memory can be extremely fast.

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Tags: 3D Stacking, Memory, Micron, Samsung

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Comments

One Response to “Samsung, Micron Unveil 3D Stacked Memory And Logic”

1. *Russell Fish* Says:
   October 31st, 2011 at 2:59 pm

   There is a way easier and less expensive technique to reducing power. Build CPUs directly on the DRAMs.

   Russell Fish
   Venray Technology

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