Micron, Samsung seek hybrid memory spec

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Micron Technology and Samsung Electronics announced the formation of an open consortium around hybrid memory cube, a technology that brings DRAM memory and logic processes together into one package to offer potential power efficiency, bandwidth, density and scalability advantages over traditional DRAM. SAN FRANCISCO—Micron Technology Inc. and South Korea's Samsung Electronics Co. Ltd. Thursday (Oct. 6) announced the formation of an open consortium around hybrid memory cube (HMC), a technology that brings DRAM memory and logic processes together into one package to offer potential power efficiency, bandwidth, density and scalability advantages over traditional DRAM.

The goal of the Hybrid Memory Cube Consortium is to establish HMC as a new memory standard, according to Micron and Samsung. The consortium will begin meeting this month to develop a specification, which they expect to be released in 2012, the companies said.

The group plans to share an early draft of an HMC interface specification with OEMs, ASIC developers and other firms at an early point for review, discussion and development, according to Scott Graham, general manager of DRAM marketing at Micron. Graham said additional HMC Consortium members would be announced later this year.

"We fully expect that there will be additional developers comprised of OEMs and enablers who will essentially be guiding the development of this spec," Graham said.

HMC relies on through-silicon-vias (TSVs)for three-dimensional stacked layers of memory with interconnect that increases performance and lowers power consumption. It also incorporates a logic layer that allows for multiple configurations for scalable bandwidth and the design flexibility for HMC to be implemented on multiple platforms, across many applications, according to Micron and Samsung. The technology also promises wide, high-speed local buses for data movement, advanced memory controller functions, DRAM control at memory, reduced memory controller complexity and increased efficiency, according to the companies.

In February, Micron introduced HMC's ability to integrate DRAM and logic processes together in one package. The current HMC platform—demonstrated last month—has validated that it can run at 128 FB/s, providing significant bandwidth, density and energy efficiency improvements, according to Micron.

Micron and Samsung believe that HMC has the potential to deliver significant improvements for applications ranging from networking and data center to consumer products such as media tablets and cards. HMC also represents a fundamental shift from current memory architectures, and driving its integration and adoption as an open standard will be a major undertaking, the companies said.

Graham said the companies believe that HMC will have the greatest near-term impact in areas where performance and energy efficiency are most critical, such as networking and high-performance computing. But ultimately the companies believe the technology will be adopted into a wide-variety of wireless, medical, energy, transportation and security devices, he said.

Graham described HMC as a response to significant challenges facing traditional DRAM, including the so-called "memory wall" created by the inability of DRAM vendors to march the performance improvements of processors. As a result, memory has become a significant bottleneck for system performance, he said.

"The CPUs are capable of processing a lot more information than the DRAM is able to deliver," said Pablo Temprano, director of DRAM marketing at Samsung Semiconductor.

In response to the disparity between the speed of processors and memory, engineers introduced a hierarchy of cache memory that is capable of running at processor clock speeds, according to Graham. But with the advent of multi-core, multi-

threaded processors, the memory needs of computational algorithms sometimes exceed the capacity of the processor cache, he said.

HMC offers the potential to alleviate this bottleneck, according to Graham and Temprano. A single HMC unit can provide more than 15 times the bandwidth of a DDR3 module and offer significant improvement in response to a random request stream, reducing system latency, they said.