

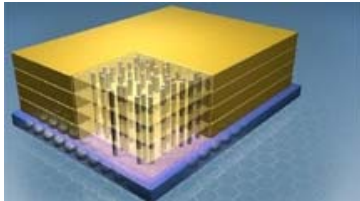


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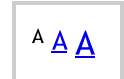
Monday, January 23, 2012



### Top Stories



## Micron & Samsung Form Hybrid Memory Cube Consortium



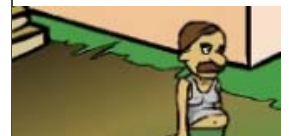
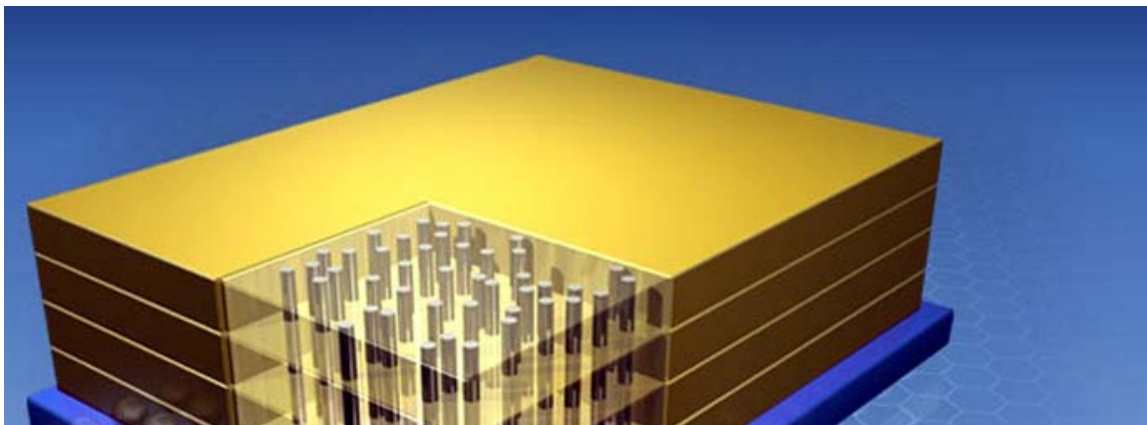
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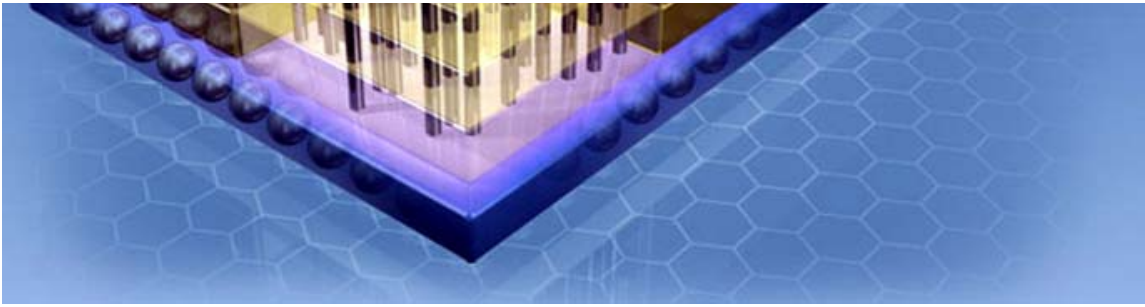
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Seems the boys in Boise have their eyes set on establishing the [Hybrid Memory Cube](#) as an industry standard. In a joint announcement today Samsung and [Micron](#) announced the formation of [Hybrid Memory Cube Consortium](#) [HMCC] whose aim is the development and implementation of an open interface specification for the technology.

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### Games





Hybrid Memory Cube is consisted out of logic layer (blue layer, with connecting BGA array), and multiple DRAM dies stacked on top of each other. Imagine an 4Gbit DRAM chip becoming 16Gbit one, and a single DIMM module with 32GB instead of current maximum of 8GB.

Micron and Samsung are the founding partners and will collaborate closely with fellow developers [Altera Corporation](#), [Open Silicon, Inc.](#), and [Xilinx, Inc.](#) to accelerate industry efforts in bringing to market a broad set of technologies. The consortium will initially define a specification to enable applications ranging from large-scale networking to industrial products and high-performance computing.

**Memory Wall**

A primary industry challenge is the need for lower latency, higher bandwidth and lower power memory than the existing infrastructure can provide. The consortium aims to break the so called "memory wall" by utilizing a hybrid approach to satisfy these requirements.

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Welcoming Matt B

On the behalf of BSN, we welcome to Matt Brodnick will be heading news and fidelity world of audio while his top secret audio lab in In any case, Matt - welcome what are you getting your: The BSN\* Team





### **Theory becomes a reality: Hyper Memory Cube achieving 128GB/s of bandwidth per chip**

As reported previously by BSN\*, a [level one demonstrator was shown in September at the Intel Developer Forum](#) streaming 128 GBytes/second. The story so far is Micron designed a 1 Gigabit [DRAM](#) with a high bank number; a smaller than 4K page size; and uses through-silicon-via [TSV] technology to bond-out a connection of a stack of four dies to a bottom logic device. This is the sum total of information released so far. A kind of [technology](#) teaser to build up the "buzz" so that media types will at the very least read their press releases.

#### **BSN\*'s Read**

This is an important component of Micron's [and Intel's] plan to realize the HMC as a high-end industry standard commodity. What is interesting is Intel's name is not on the list.

Intel's absence is the problem with this picture. Intel has long been an active participant if not the lead player in memory standards. Why have they suddenly gone missing? The memory industry needs user input to get anything that resembles a solution. There is some speculation that Intel is playing a low profile role at this point to allow other potential members a less intimidating approach to membership. There are also rumors that Intel has lost interest in the HMC technology.

Without major CPU [manufacturers](#), the consortium will have an extremely difficult time in establishing the HMC as an industry standard. Anyone remember the SLDRAM Consortium...?

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