Micron and Samsung Intend to Standardize Hybrid Memory Cube Solutions

Hybrid Memory Cubes May Become New Memory Standards

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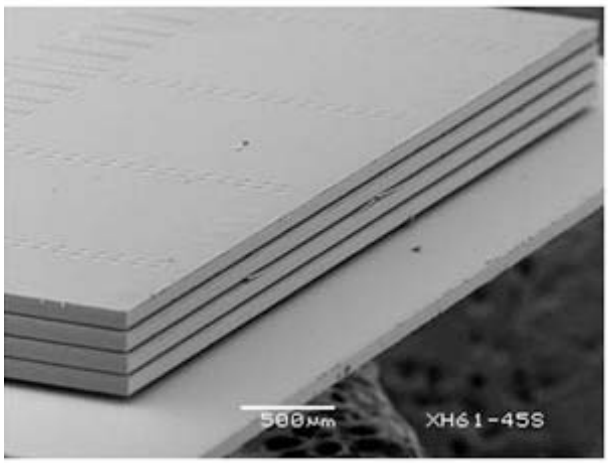
Samsung Electronics and Micron Technology, both among the largest memory makers in the world, have created a consortium for OEMs, enablers and integrators that will collaborate in developing and implementing an open interface specification for an innovative new memory technology called the hybrid memory cube (HMC).

Micron and Samsung are the founding members of the hybrid memory cube consortium (HMCC), and will work closely with fellow developers Altera Corp., Open- Silicon and Xilinx to collectively accelerate industry efforts in bringing to market a broad set of technologies. The consortium will initially define a specification to enable applications ranging from large-scale networking to industrial products and high-performance computing.

One of the primary challenges facing the industry – and a key motivation for forming the HMCC – is that the memory bandwidth required by high-performance computers and next- generation networking equipment has increased beyond what conventional memory architectures can provide. The term “memory wall” has been used to describe the problem.

Breaking through the memory wall requires a new architecture that can provide increased density and bandwidth at significantly reduced power consumption. HMC capabilities are a leap beyond current and near-term memory architectures in the areas of performance, packaging and design efficiencies. By defining an industry interface specification for developers, manufacturers and architects, the consortium is committed to making HMC a successful new high-performance memory technology.



Intel Corp. demonstrated HMC at Intel Developer Forum in September, 2011. The Hybrid Memory Cube – which was jointly designed by Intel and Micron – demonstrates a new approach to memory design delivering a 7-fold improvement in energy-efficiency over today's DDR3. Hybrid Memory Cube uses a stacked memory chip configuration, forming a compact "cube", and uses a new, highly efficient memory interface which sets the bar for energy consumed per bit transferred while supporting data rates of 1Tb/s (one trillion bits per second). This research technology could lead to dramatic improvements in servers optimized for cloud computing as well as ultrabooks, televisions, tablets and smartphones.

"This collaborative industry effort will serve as an accelerator for highly promising technology that will benefit the entire industry. The consortium will help to bring about a game-changing system solution for system designers and manufacturers that is expected to outperform memory options offered today," said Jim Elliott, vice president of memory marketing and product planning at Samsung Semiconductor.

HMC could lead to unprecedented levels of memory performance and facilitate new applications in networking, medical, energy, wireless communications, transportation, security and other markets. For example, the development of systems and technologies will enable a more efficient, reliable and secure smart grid infrastructure with integrated renewable energy resources.

"HMC is unlike anything currently on the radar. HMC brings a new level of capability to memory that provides exponential performance and efficiency gains that will redefine the future of memory. Guidance by the industry consortium will help drive the fastest possible adoption of the technology, resulting in what we believe will be radical improvements to computing systems," said Robert Feurle, Micron's vice president for DRAM marketing.

The HMCC's memory specifications will be co-developed among the consortium members. The consortium is open to an unlimited number of adopters, with the opportunity to receive early access to draft specifications and participate in specification discussions and development.