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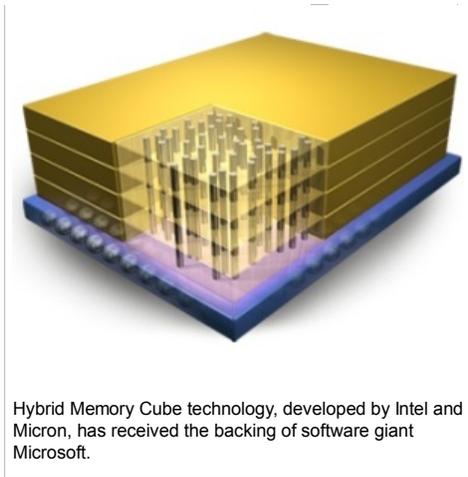
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Microsoft backs Hybrid Memory Cube tech

Published on 9th May 2012 by Gareth Halfacree

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The Hybrid Memory Cube Consortium, a group of memory industry giants led by Micron and Samsung, has announced a new member: software behemoth Microsoft.

The Hybrid Memory Cube (HMC) technology espoused by the group is a planned implementation of through-silicon via (TSV) technology - vertical conduits through a chip's silicon infrastructure which allows components to be placed in a three-dimensional mesh rather than in a traditional planar manner - which promises to dramatically improve the performance of future memory modules.

Prototypes shown off by Micron earlier this year have already proved more than capable of taking over from traditional DRAM components, showing peak throughput of 128GB/s compared to the 12.8GB/s from commercial-grade DDR3 modules created on a planar process.

Hybrid Memory Cube technology, developed by Intel and Micron, has received the backing of software giant Microsoft.

It's not all about performance, however: the process also promises dramatic power savings for mobile gadgets, with Micron's prototype modules showing a 70 per cent reduction in power draw during data transfer in a module one-tenth the size of current-generation technologies.

The technology is impressive enough to have won a stack of awards, including the Linley Group's Best New Technology Award in its 2011 round-up. Thus far, however, it is notable in its absence from the commercial markets. While there is no timescale available on when the product may launch, the fact that Microsoft is showing an interest suggests it's not too far away from becoming a commercial reality.

'*HMC technology represents a major step forward in the direction of increasing memory bandwidth and performance, while decreasing the energy and latency needed for moving data between the memory arrays and the processor cores,*' claimed Microsoft's general manager of strategic software/silicon architectures KD Hallman in an announcement to press. '*Harvesting this solution for various future systems could lead to better or novel digital experiences.*'

The Hybrid Memory Cube Consortium has indicated that, in partnership with companies including Altera, IBM, Open-Silicon, Xilinx and Microsoft, the draft interface specification for HMC memory will be ready in the very near future with a final specification due by the end of the year.

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John_T   9th May 2012, 16:00

Ten times the performance, one tenth the physical size, and 70% less power.

Is that all? :)

When they eventually start producing 3D processors, that will be truly mind-boggling!

Fizzban   9th May 2012, 16:56

mo2580   10th May 2012, 00:00

i once heard about dna processors 10 years ago and then nothing, does anybody what those were about, or did i make a mistake in reading the article it was a long time ago and i just skimmed read it.

fluxtatic   10th May 2012, 06:05

> Quote:
>
> Originally Posted by **Fizzban**
> I love it. Never been a better time to be alive, technology-wise, than now. We want moar!

I agree, but isn't that always the case for any given point in time? At least, once the Dark Ages ages. Then again, where's my *&^%#! flying car and #$%)&! nutrition pills?!

Teelzebub   10th May 2012, 07:24

> Quote:
>
> Originally Posted by **mo2580**
> i once heard about dna processors 10 years ago and then nothing, does anybody what those were about, or did i make a mistake in reading the article it was a long time ago and i just skimmed read it.

Nope, I saw a program about that years ago never seen or heard any more about it since.

Showerhead   10th May 2012, 09:22

> Quote:
>
> Originally Posted by **mo2580**
> i once heard about dna processors 10 years ago and then nothing, does anybody what those were about, or did i make a mistake in reading the article it was a long time ago and i just skimmed read it.

Not really practicle as it would take ages to set up to solve one computation and each run of the processor would only solve one problem before you had to recode the entire thing.

Would only reallly be practicle for a massively parallel task.

mingemuncher   11th May 2012, 02:36

> Quote:
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> Originally Posted by **Showerhead**
>
> > Quote:
> >
> > Originally Posted by **mo2580**
> > i once heard about dna processors 10 years ago and then nothing, does anybody what those were about, or did i make a mistake in reading the article it was a long time ago and i just skimmed read it.
>
> Not really practicle as it would take ages to set up to solve one computation and each run of the processor would only solve one problem before you had to recode the entire thing.
>
> Would only reallly be practicle for a massively parallel task.

mmmmm, synthetic dna has been developed, where multiple streams of i/o can be achieved, its the accuracy of

sdna that attracts devs, zero errors...

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