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ARM/HP/SK hynix Join Micron/Samsung Collaboration for Hybrid 3D Memory Cube (HMC) Technology

Quote

Last	Change / Per Change		
27.73	**-0.49/-1.73636 %** ▼		
Open	**High**	**Low**	**Prev Close**
27.62	27.92	27.59	28.22
Volume	**Avg Vol**	**Last Trade**	
1,853,836	2,468,422	09/24/12 16:00:00 EDT	

Consortium to Accelerate Dramatic Advances in Memory Technology Announces New Members

ARM, HP and SK hynix Join Collaboration for Hybrid Memory Cube (HMC) Technology

BOISE, Idaho, June 27, 2012

The Hybrid Memory Cube Consortium (HMCC), led by Micron Technology and Samsung Electronics Co., Ltd., today announced that new members ARM, HP, and SK hynix, Inc. have joined the global effort to accelerate widespread industry adoption of Hybrid Memory Cube (HMC) technology. The HMCC is a collaboration of original equipment manufacturers (OEMs), enablers and integrators who are cooperating to develop and implement an open interface standard for the innovative new memory technology.

Micron and Samsung, the initial developing members of the HMCC, are working closely with Altera, IBM, Microsoft, Open-Silicon, Xilinx and now ARM, HP and SK hynix â€" to draft an industry-wide specification that should pave the way for a wide range of electronic advances.

"The strong collection of companies who have joined the consortium â€" representing a broad range of technology interests â€" reflects the perceived high value of HMC as the next standard for high-performance memory applications," said Robert Feurle, Micron's vice president for DRAM marketing. **"With the addition of ARM, HP and SK hynix as developers, who will help to determine the specific features, the consortium is well positioned to provide a new open standard for next-gen electronics."**

HMC features will enable highly efficient memory solutions for applications ranging from industrial products to high-performance computing and large-scale networking. The HMCC's team of developers plans to deliver a draft interface specification to the growing number of "adopters" joining the consortium. Then, the combined team of developers and adopters will refine the draft and release a final interface specification, currently targeted for the end of this year.

As envisioned, HMC capabilities will leap beyond current and near-term memory architectures in the areas of performance, packaging and power efficiencies, offering a major alternative to present memory technology.

One of the primary challenges facing the industry -- and a key motivation for forming the HMCC -- is that the memory bandwidth required by high-performance computers and next-generation networking equipment has increased beyond what conventional memory architectures can provide. The term "memory wall" has been used to describe this challenge. Breaking through the memory wall requires architecture such as HMC that can provide increased density and bandwidth with significantly lower power consumption.

Adopter membership in the HMCC is available to any company interested in joining the consortium and participating in the specification development. Already, the HMCC has responded to interest from more than 90 prospective adopters.

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Additional information, technical specifications, tools and support for adopting the technology can be found at www.hybridmemorycube.org.

About the HMCC

Founded by leading members of the world's semiconductor community, the Hybrid Memory Cube Consortium (HMCC) is dedicated to the development and establishment of an industry-standard interface specification for the Hybrid Memory Cube technology. Members of the consortium include Altera, ARM, HP, IBM, SK hynix, Micron, Microsoft, Open-Silicon, Samsung, and Xilinx. More than 90 prospective adopters are exploring consortium membership. To learn more about the HMCC, visit www.hybridmemorycube.org.

Reply to ARM / Micron

15 X performance hybrid_3D ARM CPU/GPU/ASIC RAM Cube@70% cent less power.. Samsung/Micron/Altera/Open Silicon/Xilinx

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Not-particularly-cube-shaped cubes prove faster

By Chris Mellor â€¢ Get more from this author

Posted in PCs & Chips, 7th October 2011 15:05 GMT

We're hitting a memory wall, if you didn't know, and processor cores are going to be held up because DRAM can't scale up enough or ship 'em data fast enough. Samsung and Micron aim to fix that with 3D memory cubes and a consortium to define an interface spec for them.

Samsung and Micron, asserting that existing 2D DRAM architectures can't scale enough to meet the needs of higher and higher performance processors and graphics in computers and network equipment, have formed a HMC consortium (HMCC) to specify a standard cube interface. Other members are Altera, Open Silicon and Xilinx. Any adopter, OEM, enabler or integrator is free to join.

The key to this is the Hybrid Memory Cube (HMC), stacked layers of DRAM, on top of a foundation logic layer, interconnected by vertical pathways, Through Silicon Via (TSV) bonds, resulting in denser memory modules. **The two reckon that a single 3D cube has 15 times the performance of a single DDR3 DRAM module, while using up to 70 per cent less energy per bit**.

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The consortium members expect memory cubes to be tightly coupled with CPUs, GPUs and ASICs in point-to-point configurations.. It will provide tools and documentation to describe interface specifications as they develop and help their use. The spec should be delivered next year.

More@...http://www.theregister.co.uk/2011/10/07/hybrid_memory_cube_consortium/

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