ARM, HP and SK Hynix Join Hybrid Memory Cube Consortium

Another Three Technology Leaders to Work on HMC Memory Tech

by **Anton Shilov**
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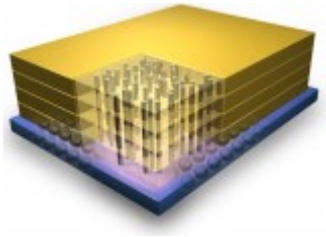
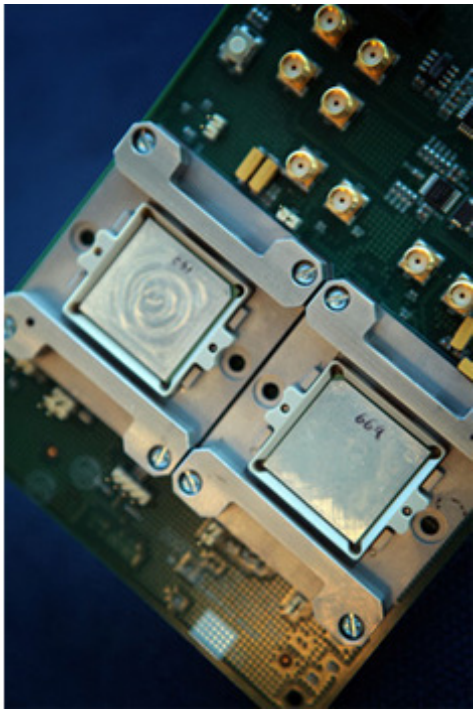


The Hybrid Memory Cube Consortium (HMCC) on Wednesday announced that new members ARM, Hewlett-Packard, and SK Hynix have joined the effort to accelerate widespread industry adoption of hybrid memory cube (HMC) technology. The new members will help to standardize HMC for different devices, from ultra-mobile products powered by ARM to mission-critical servers made by HP.

Micron and Samsung, the initial developing members of the HMCC, are working closely with Altera, IBM, Microsoft, Open-Silicon, Xilinx and now ARM, HP and SK Hynix - to draft an industry-wide specification that should pave the way for a wide range of electronic advances. With Micron, Samsung and SK Hynix aboard, it is safe to say that the key DRAM makers are now behind the HMC. With IBM and HP, it becomes apparent that high-end server system designers are also behind HMC. ARM is yet the only microprocessor technologies designer behind HMC, but keeping in mind that Intel was the first company to demonstrate the technology, it is likely that it will also support hybrid memory cube eventually.

"The strong collection of companies who have joined the consortium - representing a broad range of technology interests - reflects the perceived high value of HMC as the next standard for high-performance memory applications. With the addition of ARM, HP and SK Hynix as developers, who will help to determine the specific features, the consortium is well positioned to provide a new open standard for next-gen electronics," said Robert Feurle, Micron's vice president for DRAM marketing.



The Hybrid Memory Cube – which was jointly designed by Intel and Micron – demonstrates a new approach to memory design delivering a 7-fold improvement in energy-efficiency over today's DDR3. Hybrid Memory Cube uses a stacked memory chip configuration, forming a compact “cube”, and uses a new, highly efficient memory interface which sets the bar for energy consumed per bit transferred while supporting data rates of 1Tb/s (one trillion bits per second). This research technology could lead to dramatic improvements in servers optimized for cloud computing as well as ultrabooks, televisions, tablets and smartphones.

The HMCC's team of developers plans to deliver a draft interface specification to the growing number of "adopters" joining the consortium. Then, the combined team of developers and adopters will refine the draft and release a final interface specification, currently targeted for the end of this year.