Denali Memory Report

Market Analysis and Trends in the Semiconductor Memory Industry

ARM, HP, and SK hynix join Hybrid Memory Cube Consortium (HMCC). First spec due by end of year

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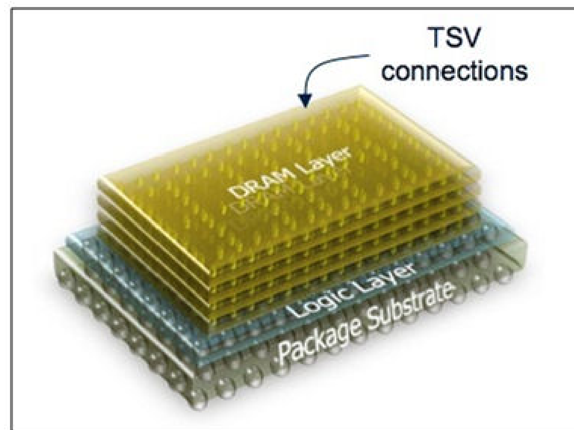
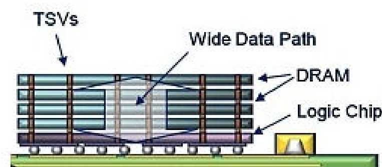
Add ARM, HP, and SK hynix to the growing list of companies in the Hybrid Memory Cube Consortium (HMCC). The three new members join the original founding companies, Micron and Samsung, along with Altera, IBM, Microsoft, Open-Silicon, and Xilinx plus a host of Adopter companies including Cadence.





I first covered the Hybrid Memory Cube in the **EDA360 Insider** nearly a year ago. (See "3D Thursday: Micron's 3D Hybrid Memory Cube delivers more DRAM bandwidth at lower power and in a smaller form factor using TSVs" and "Want to know more about the Micron Hybrid Memory Cube (HMC)? How about its terabit/sec data rate?") Just in case you weren't reading my blog back then or have forgotten, I wrote:

"Micron expects its HMC module to achieve and exceed 128 Gbytes/sec. That's at least 6x what's expected of DDR4. The only way to do that is through parallelism. The first step in exposing DRAM parallelism through the HMC is to configure each DRAM die as a 16-slice device with sixteen independent I/O ports on each die."

And this:

"The Micron HMC project illustrates why memory is a killer 3D app. With the bandwidths made possible by employing the large number of I/Os made possible through TSV interconnect, much more of the potential bandwidth available from all of those DRAM banks that have been on memory die for decades can finally be brought out and used to achieve more system performance. This is especially important in a world that increasingly makes use of multicore processor designs. Multiple core processor chips have insatiable appetites

for memory bandwidth and, as the Micron HMC demonstrates, 3D assembly is one way to achieve the required memory bandwidth."

Last December, IBM jumped on board as reported by Marc LaPedus, see "IBM, Micron Tip Foundry Deal for 3D DRAM Scheme"

Then in March, Micron discussed more details at Design West in San Jose. At that time, Micron disclosed that it had built a working prototype of the Hybrid Memory Cube that delivered 121Gbytes/sec. Not bad for a first-off prototype.

The HMCC is working on a draft of the interface spec for the Hybrid Memory Cube and plans to release a final version by the end of this year.

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