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# Hybrid Memory Cube Moves Forward

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July 2012 - The Hybrid Memory Cube Consortium has made substantial progress in the past year since its launch. The advanced memory architecture solution has now completed and locked the 10 member companies of the core development team as of the end of May 2012. They have also finalized agreements with 35 adopter companies and are processing an additional 75-80 requests for being

non-voting adopters of the technology.

The voting members of the development team - which now consists of Altera, Samsung, Micron, IBM, Open Silicon, Microsoft, Xilinx, SK Hynix, ARM and HP - is working on a draft version of the product specification which is being planned for release in Jan 2013. Currently, licensed adopters are the only ones allowed to track the progress of the specification development by the core team.

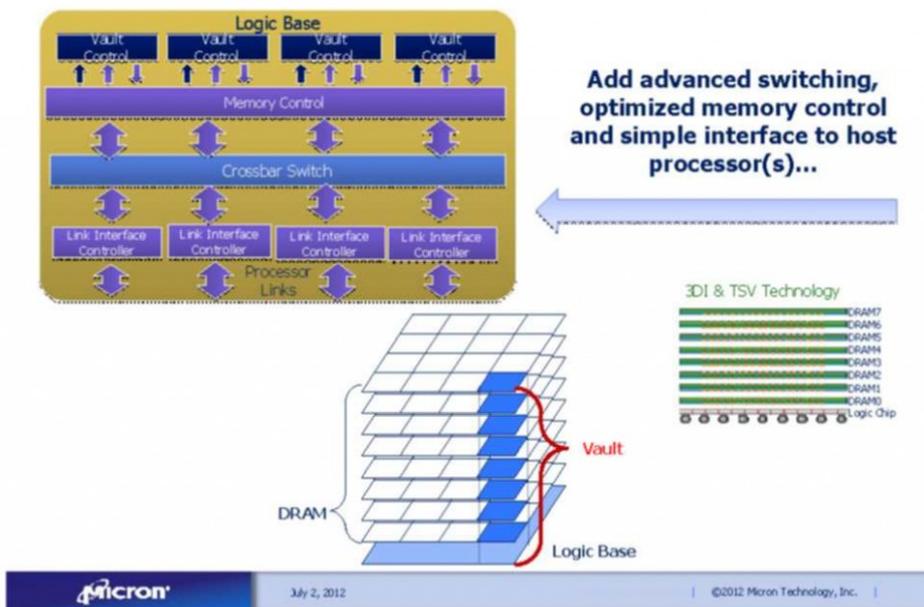
The specification will be defining an initial topology and use for the module in complete form, and define acceptable extensions for alternate topology uses and applications. These will include power and energy management, the PHY spec for the device, and logic function requirements for both near and far memory applications. The details of the logic required to implement the design are vendor specific and will vary based on process technology for the logic, but will all conform from on an interface and functional basis. This specification will also address 3D assembly and test of the product from KGD (known good die) and TSV (thru silicon via) technology. For proper operation, the final product will have a fully tested implementation including BIST (built in self test).

### Micron Hybrid Memory Cube Architecture

Micron indicated they were going to be releasing a full specification compliant product in Q2 of 2013, in the event the spec is finalized by the end of Q4 2012. The initial part will be a 2GB memory cube that is built using 4Gb DRAM array die. The product should provide about 160GBps of I/O at a 73%-85% power reduction level versus DDR3 and DDR4 solutions. This solution will so feature an almost 90% pin count reduction - 65 pins for HMC vs 600 pins for a 4 channel DDR3 solution.

The HMC solution is targeting High Performance Server Applications, as well as low power and low latency requirement applications. As VMs are becoming a critical part of the server

## HMC Architecture



application space, Mike Black Micron's chief strategist for the HMC products provided this comment on HMC's applicability to the server market - "While initial system design activity is more evolutionary in nature, with HMC providing high bandwidth memory for direct support to host processors, HMC is likely to also serve as universal or shared memory in next generation system designs. In turn, HMC's enablement of tremendously higher performance capability should allow design of new approaches for system virtualization."

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Posted by [PC](#) on Tuesday, July 10, 2012 at 12:25 am

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