

latest Xilinx FPGA (Part 2 is available [here](#)). The Xilinx press release played with the definition of 3D in what was really a question of 2.5D. Practitioners and the better prepared analysts reserve the 3DIC moniker for active integrated circuit substrates stacked with interconnection provided by through silicon vias (TSV) placed vertically within working circuits.

But a true 3DIC using the definition above can be applied to the Hybrid Memory Cube or HMC. The devices are not yet in production, but the consortium including heavyweight memory makers Micron and Samsung started laying the groundwork for the technology a few years ago. A big part of ensuring the success of new technologies like HMC - revolutionary in the consortium's words - is to allow sufficient time to get several players working together and building consensus through formal or de facto standards.

Last week, the **Hybrid Memory Cube Consortium** announced its first draft of the technology's interface specification.

This first draft specification is targeted to high performance networking and industrial applications and calls upon consortium members to refine the current short-reach interconnection revision to allow ultra short-reach physical layer memory support for FPGA, ASIC and ASSP chips.

Going back to the idea of consensus and standards, this is an important milestone for the eventual adoption of the technology. There is not consensus on when the HMC or any other 3D memory will see the production floor, but the market and performance drivers for finally taking a step up are certainly starting to align.

You can read the complete press release after the break or at http://hybridmemorycube.org/files/20120813_HMC_DSRelease.pdf.

First Draft of Hybrid Memory Cube Interface Specification Released

Industry Leaders on Track to Complete Final Specification by Year End

BOISE, Idaho and San Jose, CA, August 14, 2012 – The Hybrid Memory Cube Consortium (HMCC), led by Micron Technology, Inc., and Samsung Electronics Co., Ltd., today announced that its developer members have released the initial draft of the Hybrid Memory Cube (HMC) interface specification to a rapidly growing number of industry adopters. Issuance of the draft puts the consortium on schedule to release the final version by the end of this year. The industry specification will enable adopters to fully develop designs that leverage HMC's innovative technology, which has the potential to boost performance in a wide range of applications.

The initial specification draft consists of an interface protocol and short-reach interconnection across physical layers (PHYs) targeted for high-performance networking, industrial, and test and measurement applications. The next step in development of the specification calls for the consortium's adopters and developers to refine the specification and define an ultra short-reach PHY for applications requiring tightly coupled or close proximity memory support for FPGAs, ASICs and ASSPs.

"With the draft standard now available for final input and modification by adopter members, we're excited to move one step closer to enabling the Hybrid Memory Cube and the latest generation of 28-nanometer (nm) FPGAs to be easily integrated into high-performance systems," said Rob Sturgill, architect, at Altera. "The steady progress among the consortium's member companies for

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