Hybrid Memory Cube standard completed by consortium

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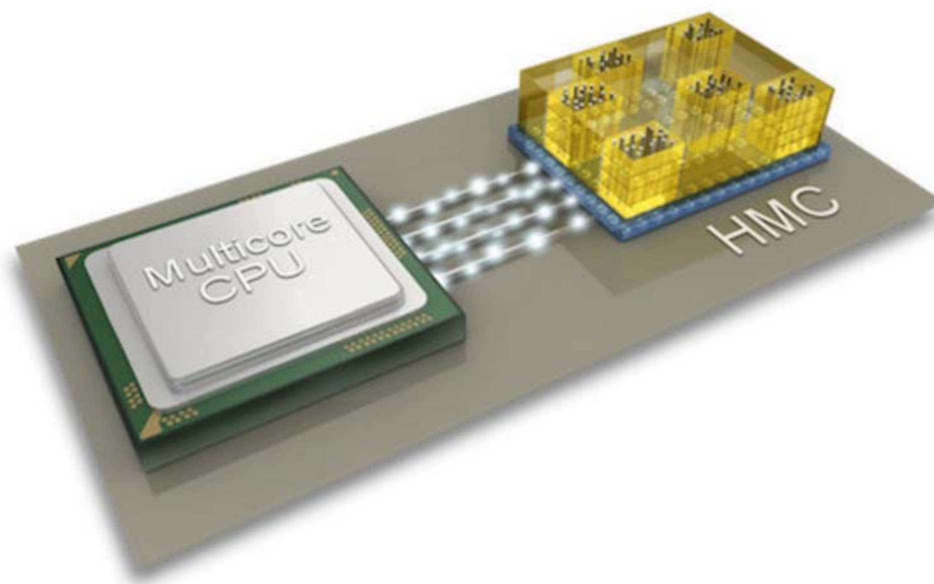
Memory bandwidth speed multiple times that of current DRAM

The Hybrid Memory Cube Consortium has published its first specification for HMC. Specification 1.0, after 17 months of work by the companies forming the consortium, details how manufacturers can create platforms and RAM using 2GB, 4GB, and 8GB chips, offering high-speed memory architectures that are also power-efficient.

HMCs use a number of memory wafers stacked on top of each other, using silicon Vertical Interconnect Access (VIAs) technology to pass electrical signal between layers.

The new specification tells of the how a HMC with eight links could hit a peak of 160Gbps of bi-directional bandwidth, writes *Computer World*. By comparison, current-generation DDR3 is capable of 11Gbps of bandwidth for communication with the processor. A blueprint for the next generation, expected to be completed by early 2014, suggests that modules with individual data link speeds of up to 28Gbps, pushing the 160Gbps figure even higher.

The first products offering the new standard are not expected to surface until later this year.



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