

[The Memory Guy](#)

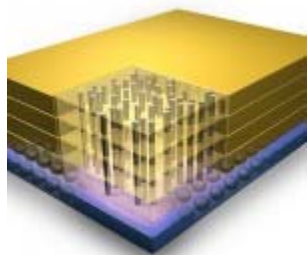
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Hybrid Memory Cube Making Progress

Published April 4, 2013 | By [Jim Handy](#)



On Tuesday the HMC Consortium (that's short for "Hybrid Memory Cube") announced that members have agreed upon a specification. The consortium has been moving rapidly, meeting its targets despite the revolutionary nature of the interface.

As a reminder, this technology stacks multiple DRAMs in a single package with a logic chip at the base of the stack that performs all the signalling to the rest of the system. Signals between the DRAMs and logic chip use through-silicon vias (TSVs) as interconnections. This allows the technology to deliver 15 times the performance of DDR3 at only 30% of the power consumption. [The Memory Guy first posted about the HMC](#) in late 2011.

The consortium explains that the HMC interface already has 100 adopters, and that a few OEMs are already evaluating conceptual prototypes. High-end servers and network switch packet buffering applications are expected to be the first adopters, followed by test and measurement applications.

The new specification adopts two interfaces, each supporting different PC board trace lengths and signalling rates:

- Short Reach: 8-10" traces, up to 15Gb/s
- Ultra-Short Reach: 2-3" traces, up to 10Gb/s

The Short Reach interface will be upgraded in a later revision, with a goal of reaching 28Gb/s, and the Ultra-Short Reach interface is aiming to get to 15Gb/s. Separate lines are used for inputs and outputs, improving throughput and allowing devices to be chained for larger memory sizes.

Micron Technology has said that it will sample a Short Reach HMC in the fall, with shipments to begin in

2014.

I see this as a very necessary step forward, that could find adoption in all computing applications by the end of the decade.

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