Wide I/O 2, Hybrid Memory Cube (HMC) – Memory Models Advance 3D-IC Standards

By Richard Goering on August 6, 2013

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Memory models are essential for SoC verification, and this week (August 6, 2013) at MemCon, Cadence is announcing the industry's first memory models for five emerging standards. This blog post provides some background about two of those standards -- **Wide I/O 2** and Hybrid Memory Cube (**HMC**) -- both of which are aimed at 3D-IC architectures. The other supported standards are **LPDDR4, eMMC 5.0**, and **LRDIMM.**

These five new memory interface standards are important because memory has become a major bottleneck with respect to performance and power goals. Specialized memory interfaces such as Wide I/O, LPDDR4, and HMC have emerged to recapture the power and performance that tomorrow's devices will demand. But you can't take advantage of these benefits without reliable memory model verification IP (VIP) that allows you to verify that your SoC works correctly with the memory that you're using.

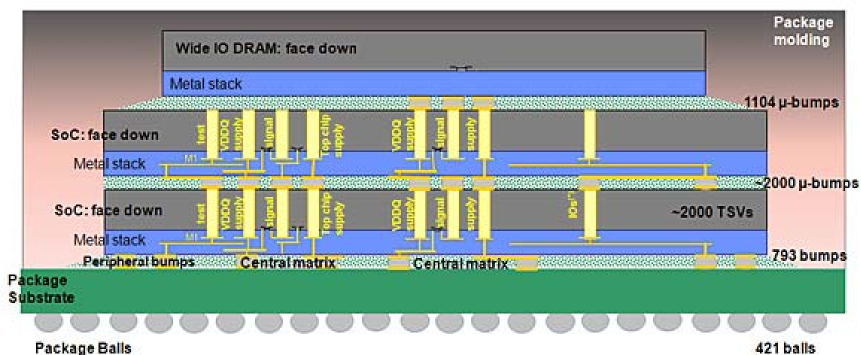
In general, Wide I/O 2 targets mobile devices while HMC aims at high-performance computing. Why support these emerging standards? "The whole memory market is moving to a 3D approach," said Scott Jacobson, senior product marketing manager at Cadence. "Whether you're in the high-performance space or a mobile space, we are supporting and helping to push these standards along."

Empowering Wide I/O 2

First, let's step back and take a quick look at the original JEDEC Wide I/O standard, published in December 2011. According to JEDEC, "Wide I/O Mobile DRAM is a breakthrough technology that will meet industry demands for increased levels of integration as well as improved performance, bandwidth, latency, power, weight and form factor." The original Wide I/O supports memory bandwidth up to 17GBps. It is aimed both at 3D die stacks with through-silicon vias (TSVs) and "2.5D" architectures where chips are placed side by side on a silicon interposer.

Wide I/O defines four 128-bit memory channels, providing a 512-bit wide interface to memory. (This is why 2.5D or 3D-IC is almost a requirement - you wouldn't want to have to route that many signals on a PCB). The interface supports a single data rate of 266M transfers/second and a channel bandwidth of 4.26GBps, for a total bandwidth of 17GBps.

In March 2011 Cadence announced the industry's first Wide I/O controller IP solution. This IP was used in an ambitious 3D-IC design project undertaken by the CEA-LETI research institute and ST-Ericsson. The project also used design tools provided by Cadence. The result was a memory-on-logic 3D stack with TSVs, as shown below and explained more fully in a previous blog post.



As time went on, many prospective users were looking for more performance and lower power than the original Wide I/O specification offered. Thus came Wide I/O 2, currently under development by JEDEC. Like the original specification, Wide I/O 2 has a four-channel architecture, but the channels have a higher bandwidth of 6.4GBps and have 64 I/Os per channel, yielding an overall 25.6GBps data rate.

Later Wide I/O 2 devices will have up to 128 I/Os per channel and a data rate of 51.2GBps. Wide I/O 2 also opens the possibility of a 1,024-bit interface to memory.

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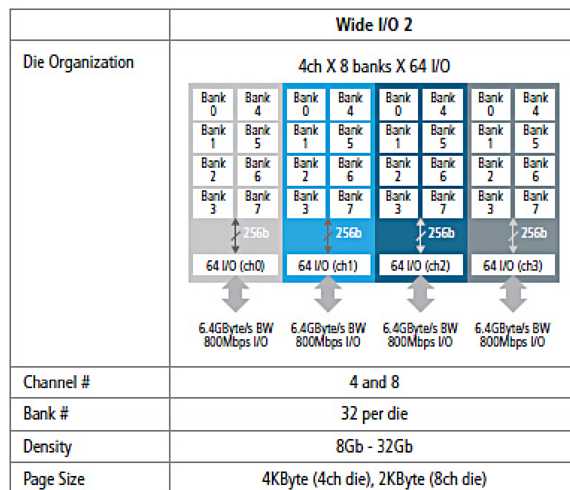


	Wide I/O 2
Die Organization	4ch X 8 banks X 64 I/O
Channel #	4 and 8
Bank #	32 per die
Density	8Gb - 32Gb
Page Size	4KByte (4ch die), 2KByte (8ch die)

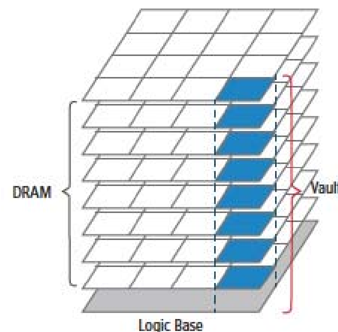
Wide I/O 2 is aimed at high-end mobile applications that require high bandwidth at the lowest possible power. The first Wide I/O 2 devices will probably be 2.5D interposer-based architectures. These take more space than 3D die stacks, but 2.5D chips also have fewer thermal problems, more flexibility to rework connections, and lower costs. Wide I/O 2 is expected to go into mass production in 2015.

Hybrid Memory Cube - Low Power, Blazing Fast

Want to go really, really fast - say, up to 320GBps? And while we're at it, how about with 70% less energy per bit than DDR3 and 90% less board space than today's RDIMMs? Then take a look at the Hybrid Memory Cube (HMC), which is expected to go into mass production in 2014.

The HMC was originally designed by Micron and is now under development by the Hybrid Memory Cube Consortium (HMCC), which is currently offering its 1.0 specification for public download and review. The HMCC includes eight "developer members" - Altera, ARM, IBM, Micron, Open-Silicon, Samsung, SK-Hynix, and Xilinx - and many "adopter members" including Cadence.

The HMC typically includes a high-speed control logic layer below a vertical stack of four or eight TSV-bonded DRAM dies. The DRAM handles data only, while the logic layer handles all control within the HMC. In the example configuration shown at right, each DRAM die is divided into 16 cores and then stacked. The logic die is on the bottom and has 16 different logic segments, with each segment controlling the DRAMs that sit on top. The architecture uses "vaults" instead of memory arrays (you could think of these as channels).



The HMC promises 15X the performance of DDR3 in addition to low power, low latency, and a small form factor. According to the HMMC web site, the HMC will "redefine memory" and could be an "absolute game changer" for applications ranging from high-performance computing to graphics. As of today, HMC is not aimed at mobile applications and is more costly than most other memory technologies.

Other New Memory Standards

In addition to Wide I/O 2 and HMC, Cadence is announcing memory model support for these emerging standards:

- **LPDDR4** - Promises 2X the bandwidth of LPDDR3 at similar power and cost points. Lower page size and multiple channels reduce power. This JEDEC standard is in balloting, and mass production is expected in 2014.
- **eMMC 5.0** - Embedded storage solution with a MMC (MultiMedia Card) interface. eMMC 5.0 offers more performance at the same cost as eMMC 4.5. Samsung announced the industry's first eMMC 5.0 chips July 27, 2013.
- **LRDIMM** - Supports DDR4 LRDIMMs (load reduced DIMMs) and RDIMMs. This standard is mostly used in computers, especially servers.

Cadence memory models support all leading simulators, verification languages, and methodologies. "We're involved early on in the standards development," Jacobson noted. "We are out there developing third-party models early. We work closely with vendors to get the models certified. If you're looking for a third-party solution for memory models, that's what we do."

Cadence memory models have a number of advanced verification and debug features that would not typically be available with in-house developed models. For more information, read this.

References

Related Blog Posts

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Three Die Stack -- A Big Step "Up" for 3D-ICs with TSVs

MemCon Keynote: Why Hybrid Memory Cube Will "Revolutionize" System Memory

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