Monday, March 03, 2014

Search | Home | News | Reviews | Articles | Guides | Download | Expert Area | Forum | Site Info

Home > News > PC Parts > Hybrid ...

Last 7 Days News : ALL | SU | MO | TU | WE | TH | FR | SA | All News

Most Popular News

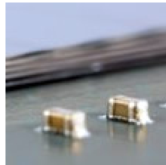
Submit your own **News** for inclusion in our Site.
Click here...

Breaking News

- Samsung's Chromebook 2 Comes In April
- Microsoft Makes Office 365 Smarter And More Social
- Bill Gates Back On Top In 2014 Forbes Billionaires List
- Samsung Galaxy S5 Buyers To Get Premium Apps For Free
- Zynga Plans New Mobile Games For March
- Google, Samsung Concerned About Microsoft-Nokia deal: report
- Chinese Windows XP Users To Get Security Support After April 8
- Toshiba Develops TransferJet-Compatible 3D-Integrated Ultra-Small Module

Tuesday, February 25, 2014

Hybrid Memory Cube Consortium Releases of Second-Generation Specification



The Hybrid Memory Cube Consortium (HMCC), dedicated to the development of an interface specification for the Hybrid Memory Cube (HMC) technology, has developed of a new interface specification.

The HMCC also released a first draft of the new specification to consortium adopters that now numbers more than 120. The new specification supports increased data rate speeds advancing short-reach (SR) performance from 10 Gb/s, 12.5 Gb/s, and 15 Gb/s, up to 30 Gb/s. The new specification also migrates the associated channel model from SR to VSR to align with existing industry nomenclature. The ultra short-reach (USR) definition also increases performance from 10 Gb/s up to 15 Gb/s.

The HMCC, founded by memory providers Micron Technology, Samsung Electronics, and SK hynix, has begun circulating this draft specification to adopters, with the goal of incorporating adopter members' input and targeting a completion date of May 2014 for the final version. The first-generation specification was completed and released publicly in April 2013; several developer and adopter companies, including Altera, Xilinx, and Open-Silicon, have already begun leveraging the specification to design products and solutions that incorporate HMC technology.

HMC uses through-silicon vias (TSVs) - vertical conduits that electrically connect a stack of individual chips - to combine high-performance logic with dynamic random access memory (DRAM) die. The first commercial HMC implementation is sampling from Micron in a 2GB density with a 160 GB/s of memory bandwidth, while using up to 70 percent less energy per bit than existing technologies.

Tweet

Active Discussions

- Made video, won't play back easily
- Questions durability monitor LCD
- Questions fungus CD/DVD Media, Some expert engineer in optical media can help me?
- CD, DVD and Blu-ray burning for Android in development
- IBM supercharges Power servers with graphics chips
- Werner Vogels: four cloud computing trends for 2014
- Video editing software.
- CD Drive Retrieve

Previous | | Next
DISNEY Debuts Digital Movie Service | All News | **MWC: Freescale Unveils Ultra-small MCU For Internet of Things Applications**
AMD and BlueStacks Bring New Dual-OS Android Solution to Retail | PC Parts News | **Toshiba Develops Accelerates Embedded NAND With New Controller**

Related News

- Micron's Hybrid Memory Cube Gets Into Supercomputers
- Micron Ships First Samples of Hybrid Memory Cube
- Hybrid Memory Cube To Boost DRAM Bandwidth
- ARM, HP and SK hynix To Participate On The Development Of Memory Cube

Home | News | All News | Reviews | Articles | Guides | Download | Expert Area | Forum | Site Info

Site best viewed at 1024x768+ - CDRINFO.COM 1998-2014 - All rights reserved -
Privacy policy - Contact Us .